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Efficient CMOS layout Design of Half Subtractor using 90nm technology

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Abstract— The subtractors are the digital circuits that are used to calculate the subtraction between two inputs or variables. The main objective of this paper is to design a 1-bit half subtractor. Three design methods are taken into consideration namely fully automatic, semicustom and full custom. In the very first approach fully, automatic design inbuilt actives are used along with auto routing and placement. In second approach, semicustom design inbuilt active devices are used along with optimized placement and manual routing. In third approach, full custom design inbuilt active layers are used along with the optimized manual device formation and manual placement and routing of the devices. In fully automatic approach proposed schematic is designed with the help of the DSCH and its equivalent layout is created using the Microwind. It is observed from the simulated results that there is 59.30% reduction in power consumption and 34.90% reduction in area in case of full custom layout design as compared to the fully automatic design.

Keywords- CMOS technology; Layout; Half subtractor; Foundries; VLSI

1. INTRODUCTION

With the advancement of various technologies in the modern world, everything is being compact and is being reduced in size. The VLSI technology is required for the reduced device sizes. For various applications the CMOS based technology is used to make the integrated circuits. The basic functional block unit of the digital system is now a day's implemented or designed using the help of the CMOS. The demands are incremented with the advancement of the technology there is advancement in use of the devices that are operated by the battery, such as notebooks, PDA's cellular phones etc. they all need compact and efficient design of these devices in such a way that power and area is efficient enough, thus to achieve the this VLSI (Very Large Scale Integration) is the technology that is needed, and ULSI (Ultra Large-Scale Integration designs) is further used to improve the time delays. For more than few years the basic digital circuit for the various applications is subtractors/adders, thus numerous researches are carried out in these fields [1, 2].

Over millions of transistors are embedded onto a single chip using the VLSI called as an integrated circuit, the IC should be scalable and energy-efficient, and for this the basic functional unit is of increased importance for the system design. The microchips utilized as a part of DSP activities e.g. in picture handling applications. Prior to the presentation of VLSI innovation, most ICs had a restricted usefulness. ICs have three key focal points over computerized circuits viz. estimate, control utilization and speed. This prompts format plan and its reproduction in order to get extremely close to an Implementable circuit outline on silicon wafer. So far a few advancements have been utilized to configuration full subtractor cell to enhance region and power utilization [3]-[8] Using the VLSI technology based on cmos design implementation the design and layout structure of the half and full subtractors are carried out and further optimization is carried out for the efficient power and area consumption of the subtractor structure.

2. SUBTRACTORS

A subtractor performs subtraction which is one of the four essential double tasks. In numerous PCs and different sorts of processors, subtractors are utilized for the number juggling figuring's, as well as every now and again utilized as a part of different parts of the processor. The subtractors can be developed to work on parallel numbers. Contingent on the utilization of the gadget or the motivation behind the application to be played out, the contributions to the circuit gadget may fluctuate from a few. We could utilize a Half-Subtractor on the off chance that we have two data sources while for three information sources; a Full-Subtractor can be utilized.

2.1. Half subtractor

A half subtractor is simplest and the most basic structure used for carrying out one bit subtraction between two binary digit

inputs and producing the two outputs weather a difference or borrow. A half subtractor consists of an AND gate having two inputs, an inverter and a XOR gate with two inputs. The output depicts weather a '1' has borrowed [9]. The subtraction can be carried out by performing the two's compliment of the number. After taking the 2's compliment the number is added with each other and the subtraction is carried out.

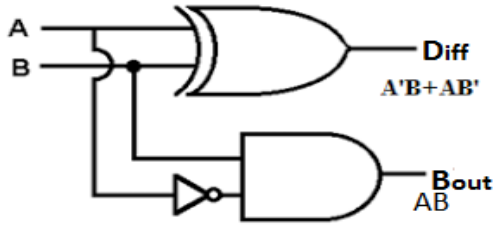

Fig.1. Conventional one bit half subtractor [2]

Fig.1. shows the circuit diagram of 1 bit subtractor having two outputs difference (Diff) and borrow (Bout). Table1 shows the truth table of the half subtractor.

Table1. Truth table

A	B	Diff(d)	B_{out}(br)
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

2.2. Full subtractor

A full subtractor is used to carry out the subtraction in between more than two input variables unlike in half subtractor. In case of three data inputs the full subtractor circuit is used. A 1 bit full subtractor can be simply made by combining two half subtractor circuits. A full subtractor has two outputs and three inputs. The functioning is carried out by the circuit by considering the previous borrow and three inputs. Fig. 2. shows the basic circuit of the full subtractor.

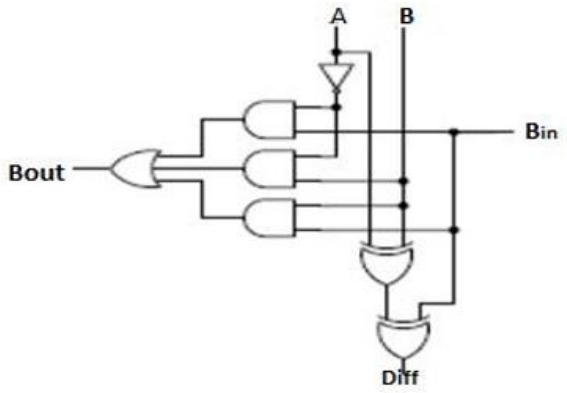

Fig.2. Conventional circuit of full subtractor

Table2: truth table of full subtractor

A	B	B_{in}(borrow)	Difference	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

From the truth table the logic expression of the full subtractor comes out to be:

Difference =A XOR B XOR B_{in} --------- (1)

Borrow out = $A'B'B_{in} + A'BB_{in}' + A'BB_{in} + ABB_{in}$ ------ (2)

$= A'B + A'B_{in} + BB_{in}$ ---------- (3)

In full subtractor when subtraction is carried out first of all two inputs are take into consideration at first minuend and subtrahend, moreover if a borrow is borrowed from the previous lower minuend is also taken into consideration. Thus this way three data sources are taken care of at the contribution of the full subtractor, to be specific two bits to be subtracted and also the borrow bit. From the truth table difference shows the subtraction output obtained by subtracting three input bits and borrow out B_{out} tells weather a borrow 1 is required by the minuend bit from the next higher minuend bit.

3. SCHEMATIC DESIGN SIMULATION

4.

Schematic design of the half subtractor circuit is made using the DSCH software; the gates are dragged and dropped from the symbol library provided in the software, the half subtractor circuit schematic circuit is made using nand gates. Fig.3. shows the schematic diagram of the half subtractor using nand gates.

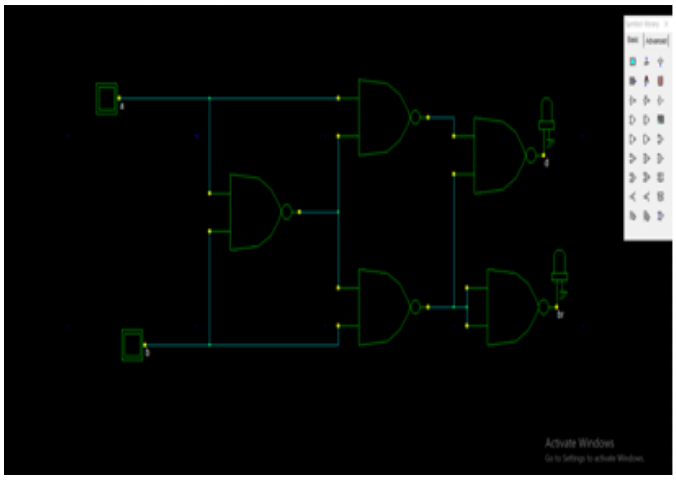

Fig.3. Schematic diagram of half subtractor

After the schematic design the simulation results are carried out, that is the output waveform is checked and is verified with the truth table of the half subtractor. Fig.4. shows the simulation result obtained by using schematic design of the circuit.

Fig.4. Output waveform of schematic design

4. LAYOUT DESIGN SIMULATION

The first method in the simulation of the half subtractor is carried out using the DSCH software. The basic circuit of the half subtractor is designed at gate level with the help of the DSCH and then further verilog file of the half subtractor circuit is created and is compiled in the Microwind software which gives us the fully automatic design of the half subtractor using CMOS Technology. The particular foundry for the CMOS design is then selected which is here is basically 90nm.Various designs of the half subtractors are compared and the basis of the power consumption and its area.

4.1. Fully automatic design

Fully automatic design layout is obtained at the cmos level on the Microwind software for this the verilog file of the schematic design is compiled in Microwind, since for the layout design the 90nm technology of the cmos is used therefore 90nm foundry is selected for the obtained fully automatic design. The clock values are assigned as per the requirement and thus the fully automatic design is carried out for the simulation process. Fig.5 shows the fully automatic layout design of the half subtractor obtained after compilation of the verilog file of the schematic design in the Microwind software. The fully automatic design is so called because it is not created manually but is developed by the software itself from the verilog file.

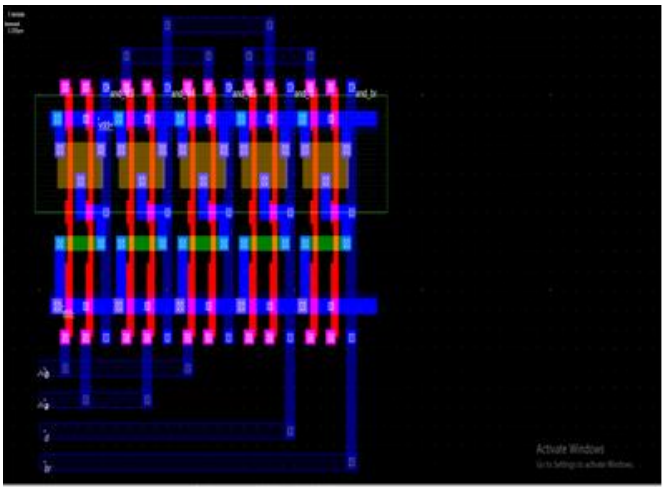

Fig.5. Fully automatic layout design of half subtractor

The design is checked for DRC (design rule check) to calculate the errors. The errors are removed if they are present. After successful compilation ad DRC check the circuit is carried out for the timing simulations, the simulation results thus obtained are verified using truth table of the half subtractor. Fig.6. shows the simulation results of the fully automatic layout design of half subtractor circuit.

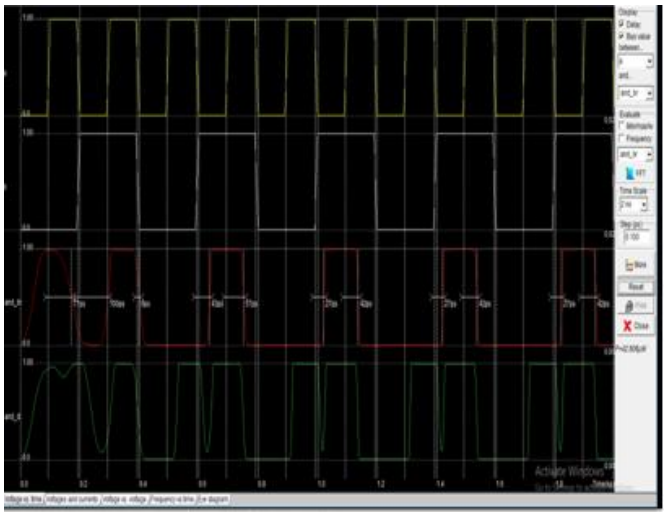

Fig.6. Output timing waveform of auto generated circuit

After the successful simulation of the auto generated half subtractor circuit in Microwind the power and area is taken into the consideration. The power consumption of the auto generated circuit is 42.808µW and area used comes out to be 40.40 μm^2.

4.2. Semicustom layout

The second approach is the semicustom design of the half subtractor which is basically used to reduce the area of the circuit form that of the previous simulation, in this approach manual designing of the circuit is carried out, lambda rules are used as a whole by the designer in manual approach. N-MOS and p-MOS devices are selected from the palette and thus the manual connection is done between them using the metal contacts and polysilicon. After providing the connection between these cmos transistors, the half subtractor circuit is made; the connection between different cmos gates are carried out using polysilicon and metal contacts. Since the polysilicon used is highly resistive in nature which would increase the power consumption of the semi custom design, thus for the lesser power consumption the metal1, and metal2 are used for the interconnections along with the polysilicon. Lesser the amount of the polysilicon used lesser will be the resistance in the circuit and hence lesser power consumption. The layout design of the half subtractor is thus completed with proper interconnections in between the different gates. The structure thus formed must be checked using the DRC function provided by the Microwind software. Fig.7. shows the semi custom layout of the half subtractor.

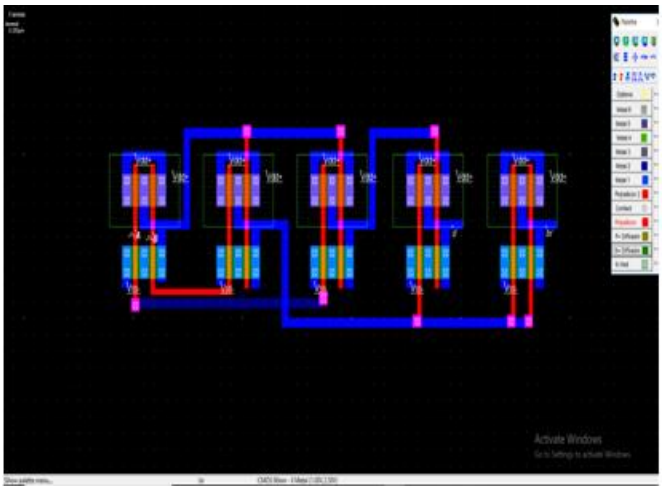

Fig.7. Semi custom layout of the half subtractor

The semi-custom layout design is checked for DRC (design rule check) which notifies as if any errors are present or not; which can be removed (if present any). Layout design is carried out for the timing simulations, which gives us the timing waveforms of the circuit and thus the timing waveform is verified using the truth table of the half subtractor. Fig.8. shows the timing simulations of the semi custom layout design of half subtractor circuit.

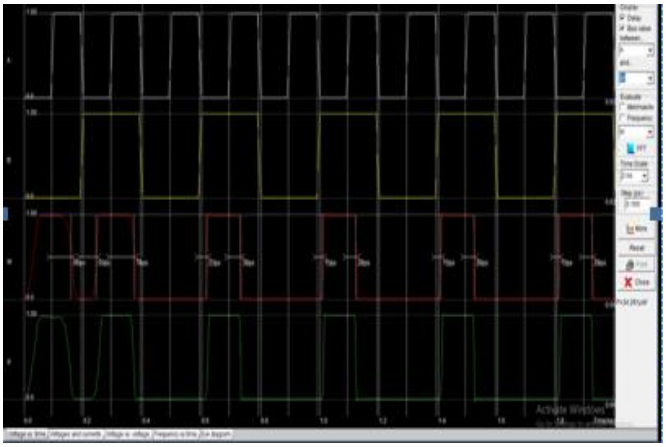

Fig.8. Output timing simulations of manual design

In semi-custom layout design the power consumption is 34.261µW and the area used by manual design is 31.8μm^2. The power consumption is reduced by 15.29% and the area coverage is reduced by 21.2% from the fully automatic layout design.

4.3. Full custom

The third approach that can be taken into consideration is the full custom approach. The full custom approach is a manual approach similar to the semicustom approach but in fully custom design the transistors are designed using the CMOS

technology, using n-diffusion, p-diffusion, n-well/p-well, polysilicon and metal contacts, and from these the structure is manually created from the starting point. All these masks and metal contacts are selected from the palette provided in Microwind.Fig.9. shows the full custom layout of the half subtractor.

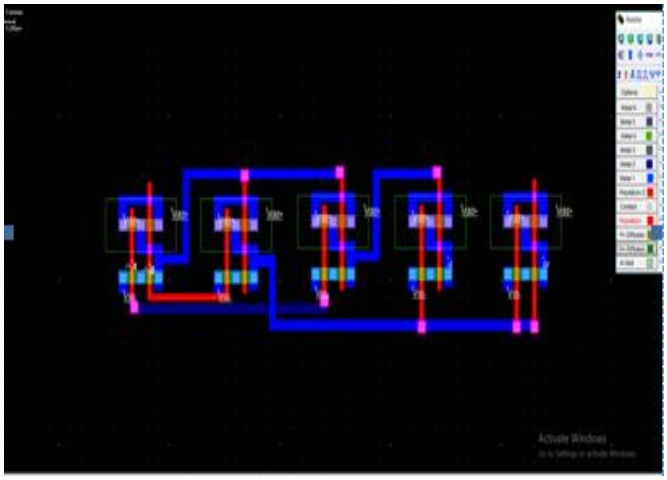

Fig.9. Full custom layout of half subtractor.

To reduce the power it is taken into the consideration that the polysilicon should be used as less as possible. Since it would provide the resistance and hence power consumption would increase. The structure made using the full custom approach is then carried out with the DRC to check if there is any error or violation of the lambda rules during the designing of the full custom design. If there is any kind of DRC error resent then the circuit is again modified. The final fully custom layout design is afterwards simulated and the timing waveforms are generated and are verified from the truth table. Fig.10. shows the timing generations of the half subtractor's full custom design.

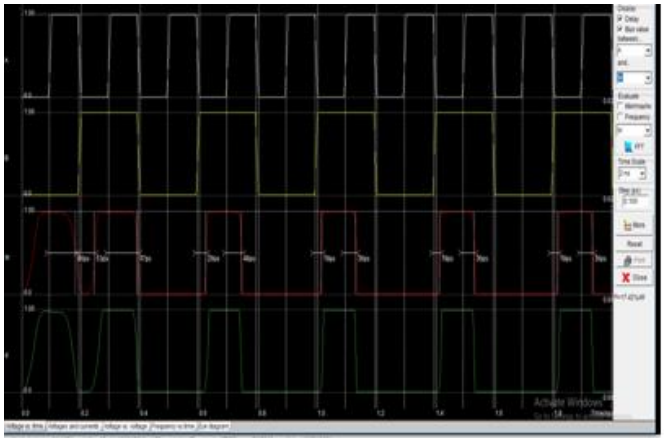

Fig. 10. Timings waveform of full custom design

In full custom layout design the power consumption comes out to be 17.421µW and the area acquired is 26.3µm^2.

5. PERFORMANCE COMPARISION

The performance comparison of the full custom and semicustom design process is taken, where the fully automatic structure is kept as the reference. Power and area are kept as the parameters for the comparison. Between the three design methods a comparative study can be carried out based upon the results obtained from these.

TABLE 3: Comparison between different layouts

S.No.	Design method	Power (µW)	Area (µm^2)
1	Auto-generated	42.808µW	40.40 µm^2
2	Semi-custom	34.261µW	31.8µm^2
3	Full-custom	17.421µW	26.3 µm^2

It is clear from the above table that the area and power consumed by the semicustom layout design is lesser than that of the fully automatic layout design. Moreover the full custom design provides the best results in terms of area and power consumption which are reduced in full custom design as compared to both fully automatic design and the semi custom layout design. Fig.11. shows the bar graph comparison in terms of area and power of the three layout designs.

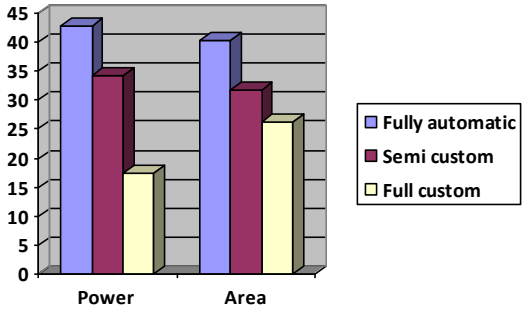

Fig.11. Bar graph of the three layout designs

As it is clear from the above bar graph minimum power and area is consumed by the full custom layout design. Further the semicustom design also consumes the lesser area and power as compared to the fully automatic design.

6. CONCLUSION

From the various analysis carried out it is clear that the semicustom design is efficient from the auto generated layout design in terms of the area and power. So, where the area

reduction is concerned the semicustom design can be implemented. In portable devices, the semicustom design has application, with the efficient area and power design. The area is reduced from 40.40µm^2 to 31.8µm^2 and power is reduced from 42.808µW to 34.261µW in semicustom from the fully automatic design layout. The full custom design however provides the best results in both the parameters, namely area and power, thus the fully custom design is the most efficient design amongst the three cmos layout designs namely semicustom; fully automatic; and the full custom layout. The area coverage is reduced from 31.8 µm^2 to 26.3 µm^2 and power consumption is reduced from 34.261 µW to 17.421 µW in full custom layout design when compared with the semicustom layout design; And when compared with the fully automatic layout design there is a reduction in area from 40.40 µm^2 to 26.3 µm^2 and from 42.808 µW to 17.421 µW reduction in the power consumption.

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